STATE INSTITUTE OF ENGINEERING &TECHNOLOGY, NILOKHERI

ANALOG CIRCUITS LAB MANUAL

List of experiments:

1. To design a simple common emitter (CE) amplifier circuit using BJT and find its gain and frequency response.
2. To design a BJT emitter follower and determine is gain, input and output impedances.
3. To design and test the performance of Phase shift Oscillator using Op-Amp 741.
4. To design and test the performance of Wien bridge oscillator using Op-Amp 741.
5. To design and test the performance of BJT – Hartley Oscillators for RF range f0 ≥100KHz.
6. To design and test the performance of BJT – Colpitt Oscillators for RF range f0 ≥100KHz.
7. To design an astable multivibrator using 555 timer.
8. To design a monostable multivibrator using 555 timer.
9. To design Schmitt trigger using Op-amp and verify its operational characteristics.
10. To design and test Operational amplifier applications: (1)Inverting Amplifier, (2) Non-Inverting Amplifier, (3) Summer, (4) Voltage Follower, (5) Integrator and Differentiator.

CONTENTS

EXPERIMENT 1
FREQUENCY RESPONSE OF CE AMPLIFIER

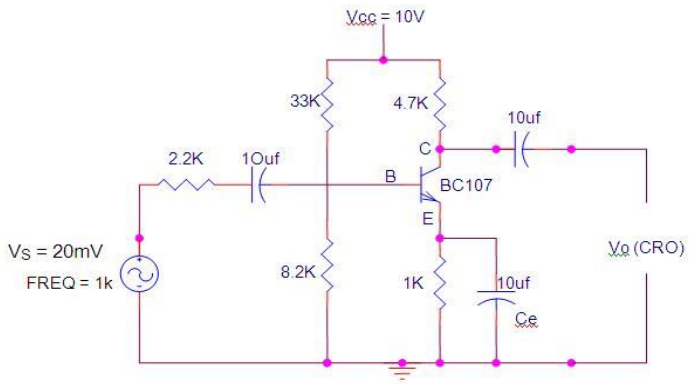
AIM To design a simple common emitter (CE) amplifier circuit using BJT and find its gain and frequency response.

APPARATUS:

S.No	Apparatus	Type	Range	Quantity
01	Transistor	BC107		01
02	Resistance		33KΩ,4.7 KΩ,2.2 KΩ 8.2 KΩ,1 KΩ	01
03	Regulated Power supply		(0-30V)	01
04	Capacitor		10µF	03
05	Signal Generator		10-1M Hz	01

06	CRO			01
07	Breadboard and Wires ,CRO Probes			

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. A 10V supply is given to the circuit.
3. A certain amplitude of input signal (say 20mv at 1 kHz) is kept constant using signal generator and for different frequencies, the output voltage (V_0) from CRO are noted.
4. Gain for with and without feedback is calculated using $Gain(dB) = 20 \log \frac{V0}{}$; Where V_o is output voltage, V_i is input voltage.
5. Plot the graph between Gain(in dB) and frequency.

TABULAR COLUMN:

S.no.	Input frequency (Hz)	o/p voltage(v_o) (mv)	voltage gain $A_v = \frac{V_0}{V_i}$	$Gain(dB) = 20 \log \frac{V_0}{V_i}$
	100Hz To 1MHz			

MODEL GRAPH:

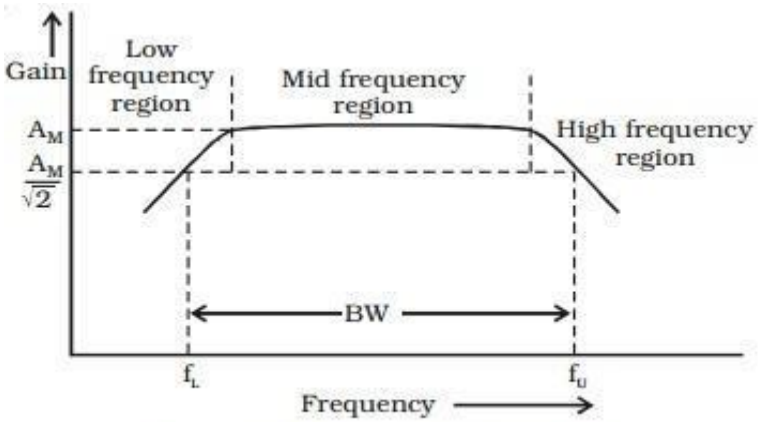


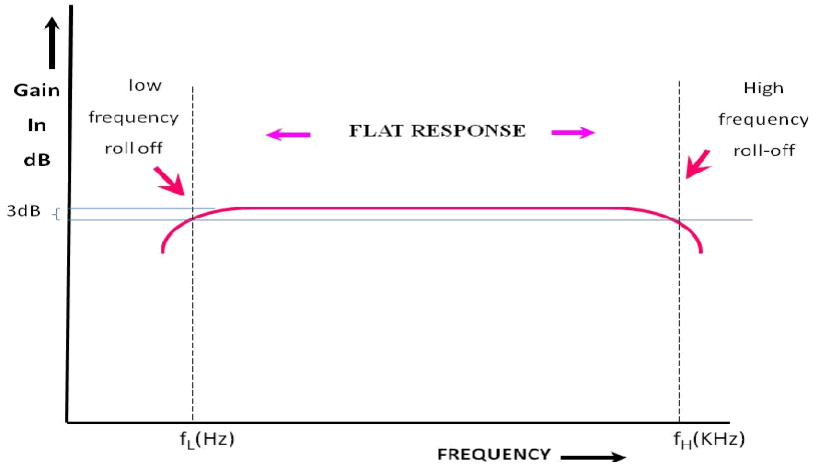
Fig Frequency response curve

Calculations from Graph

1.Draw a line at maximum gain(dB) less than by 3dB parallel to the X-axis as shown in the figure.

2 Draw two lines at the intersection of the characteristic curve and the 3dB line onto the X-axis which gives the (f_H) and (f_L)

3.The difference between f_H and f_L gives the Bandwidth of the amplifier.



PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.

2. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

3. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULT:

EXPERIMENT NO. 2
EMITTER FOLLOWER

AIM: -To design a BJT emitter follower and determine is gain, input and output impedances.

APPARATUS REQUIRED:- Transistor - BC 107, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Set V_i = 1 volt (say), using the signal generator
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz in regular steps of 10 and note down corresponding output voltage.
4. Plot the frequency response: Gain (dB) vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

Design :-

Given $V_{CEQ} = V_{CE2} = 6v$

$I_{CQ} = I_{C2} = 5mA$

Assume þ for SL100 = 100

$V_{CC} = 12v$

$$V_{E2} = \frac{V_{CC}}{2} = \frac{12}{2} = 6v$$

$$I_{E2}R_E = V_{E2}$$

$$\therefore R_E = \frac{V_{E2}}{I_{E2}} = \frac{6}{\times 10^{-3}} = 1.2k\Omega\ 5 \qquad [\ IE_2 = IC_2\ ]$$

$$\therefore R_E = 1.2k\Omega$$

$$VB_1 = VBE_1 + VBE_2 + VE_2$$

$VB_1 = 0.7 + 0.7 + 6$

$VB_1 = 7.4v$

$$IB_2 = \frac{I_{C2}}{\beta} = \frac{5\times10^{-3}}{100} = 0.05mA$$

$$IB_1 = \frac{I_{C1}}{\beta} = \frac{I_{B2}}{\beta} = \frac{0.05}{100} = 0.0005mA$$

$10IB_1R_1 = V_{CC} - VB_1$

$$\therefore R_1 = \frac{12 - 7.4}{10\times0.0005\times10^{-3}} = 920k\Omega \text{ [Use } R_1 = 1M\Omega]$$

$$R_2 = \frac{V_{B1}}{9I_B} = 1644k\Omega$$

$\therefore R_2 = 1.5M$

General Procedure for Calculation:

1. Input impedance

a. Connect a Decade Resistance Box (DRB) between input voltage source and the base of the transistor (series connection).

b. Connect ac voltmeter (0-100mV) across the biasing resistor R_2.

c. Vary the value of DRB such that the ac voltmeter reads the voltage half of the input signal.

d. Note down the resistance of the DRB, which is the input impedance.

2. Output impedance

a. Measure the output voltage when the amplifier is operating in the mid-band frequency with load resistance connected (V_{load}).

b. Measure the output voltage when the amplifier is operating in the mid-band frequency without load resistance connected ($V_{no\text{-}load}$).

c. Substitute these values in the formula $Z_{\text{o}} = \frac{V_{load} - V_{no-load}}{V_{load}} \times 100\%$

3. Bandwidth

a. Plot the frequency response

b. Identify the maximum gain region.

c. Drop a horizontal line bi –3dB.

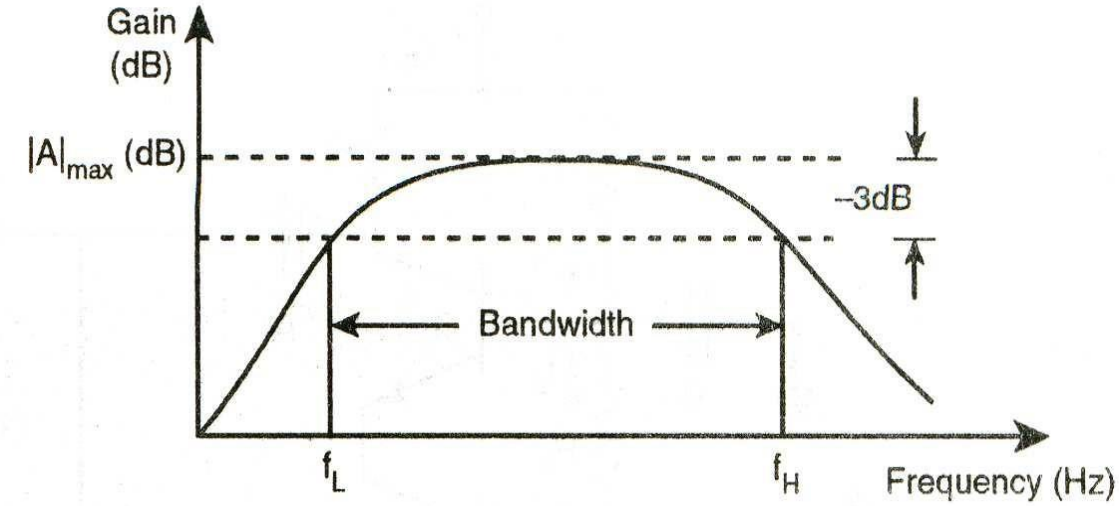
d. The –3dB line intersects the frequency response plot at two points.

e. The lower intersecting point of –3dB line with the frequency response plot gives the lower cut-off frequency.

f. The upper intersecting point of –3dB line with the frequency response plot gives the upper cut-off frequency.

g. The difference between upper cut-off frequency and lower cut-off frequency is called Bandwidth. Thus Bandwidth = $f_h - f_l$.

Model Graph: (Frequency Response)



TABULAR COLUMN: -

Sl No.	Frequency	V_O (volts)	Gain = V_O/V_i	Gain (dB) =20log V_O/V_i

4 To find Q-Point

a. Connect the circuit as per circuit diagram

b. Switch on the DC source [switch off the AC source]

c. Measure voltage at V_{B2}, V_{E2} & V_{C2} with respect to ground

& also measure

$$V_{CE2} = V_{C2} - V_{E2}$$

$$I_{C2} = I_{E2} = \frac{V_{E2}}{R_E}$$

$$Q - Point = [V_{CE2}, I_{C2}]$$

Result

	Theoretical	**Practical**
Input impedance		
Output impedance		
Gain (Mid band)		
Bandwidth		

EXPERIMENT NO-3

AIM To design and test the performance of Phase shift Oscillator using Op-Amp 741.

Apparatus Required: Design kit IC 741, CRO, connecting wires resistance (10k,3.3k x 3 ,1M variable pot,) capacitor .047uf x 3.

Circuit Diagram of RC Phase shift oscillator

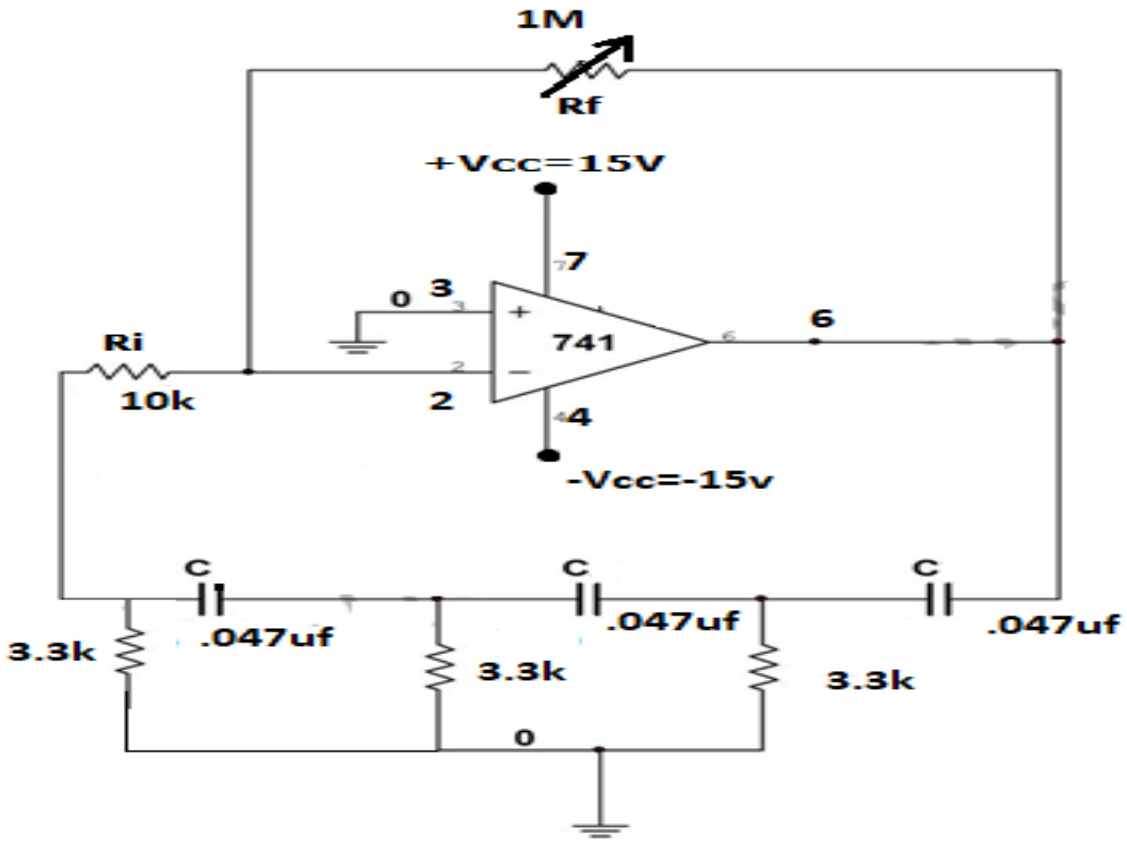


Fig: Circuit Diagram of RC Phase shift oscillator

Theory:-

RC phase shift oscillator is a oscillator consist of an op-amp as amplifier stage. it is primary used for oscillation of audio frequency (AF). It consist of rc cascaded circuit provided feedback voltage from the output back to input of amplifier. The op-amp is used in the inverting

mode, therefore inverting terminal is shifting by 180 at the output. The feedback network offers 180 degrees phase shift at the oscillation frequency and the op amp is configured as an Inverting amplifier, it also provide 180 degrees phase shift. Hence to total phase shift around the loop is 360=0degrees, it is essential for sustained oscillations. At the oscillation frequency each of the resistor capacitor filter produces a phase shift of 60° so the whole filter circuit produces a phase shift of 180°. The energy storage capacity of capacitor in this circuit produces a noise voltage which is similar to a small sine wave, it is then amplified using op amp inverting amplifier. By taking feedback, the output sine wave also attenuates 1/29 times while passing through the RC network, so the gain of inverting amplifier should be 29 in order to keep loop gain as unity. The unity loop gain and 360 degree phase shift are essential for the sustained oscillation. RC Oscillators are stable and provide a well shaped sine wave output with the frequency being proportional to 1/RC and therefore, a wider frequency range is possible when using a variable capacitor. However, RC Oscillators are restricted to frequency applications because at high frequency the reactance offered by the capacitor is very low so it acts as a short circuit.

Procedure:-

1. Connect the circuit as shown in fig.
2. To connect the DC supply +15v to pin no-7 and -15v to pin no-4 of ic741.
3. Connect CRO probe to CRO and measure the frequency of oscillator.
4. Adjust the value of feedback resistor(variable pot 1M).

Precautions:-

1. Make sure connection of circuit is proper as circuit diagram.
2. The connection should be tight.
3. Measure the output frequency exactly.

Observations:-

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

$$\text{Error \%} = \frac{\text{Theoritical frequency- practical frequency}}{\text{Theoritical frequency}} \quad \text{x } 100$$

Result :- The RC phase shift oscillator has been designed and calculated frequency of oscillator.

EXPERIMENT NO-4

AIM To design and test the performance of Wien bridge oscillator using Op-Amp 741

Apparatus Required: Design kit, CRO, Connecting wires, IC741 resistance(2 x 3.3k, 1K, 1M variable pot) ceramic capacitor (.047uf x 3).

Circuit Diagram of Wein Bridge Oscillator.

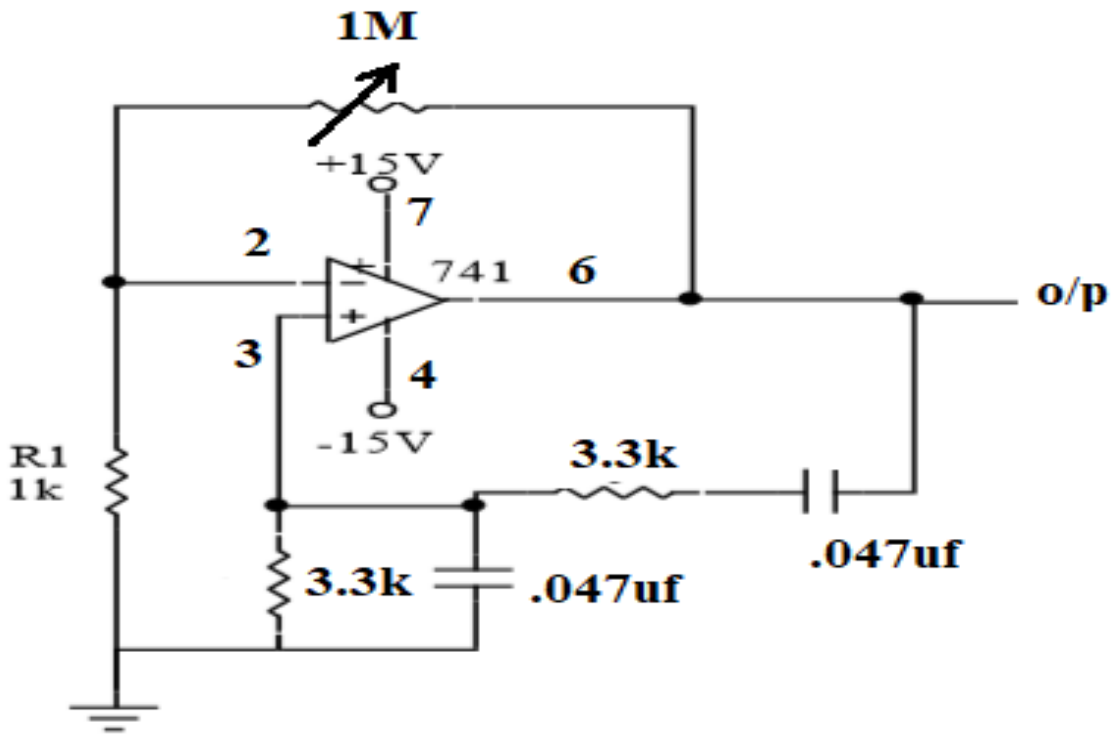


Fig. Circuit Diagram of wein Bridge Oscillator

Theory:-

The **Wien Bridge Oscillator** uses a feedback circuit consisting of a series RC circuit connected with a parallel RC of the same component values producing a phase delay or phase advance circuit depending upon the frequency. At the resonant frequency fr the phase shift is 0^o.

Consider the circuit below. The above RC network consists of a series RC circuit connected to a parallel RC forming basically a High Pass Filter connected to a Low Pass Filter producing a very selective second-order frequency dependant Band Pass Filter with a high Q factor at the selected frequency, fr. At low frequencies the reactance of the series capacitor (C1) is very high so acts a bit like an open circuit, blocking any input signal at Vin resulting in virtually no output signal, Vout. Likewise, at high frequencies, the reactance of the parallel capacitor, (C2) becomes very low, so this parallel connected capacitor acts a bit like a short circuit across the output, so again there is no output signal. So there must be a frequency point between these two extremes of C1 being open-circuited and C2 being short-circuited where the output voltage, V_{OUT} reaches its maximum value. The frequency value of the input waveform at which this happens is called the oscillators *Resonant Frequency*, (fr). At this resonant frequency, the circuits reactance equals its resistance, that is: Xc = R, and the phase difference between the input and output equals zero degrees. The magnitude of the output voltage is therefore at its maximum and is equal to one third (1/3) of the input voltage as shown. It can be seen that at very low frequencies the phase angle between the input and output signals is "Positive" (Phase Advanced), while at very high frequencies the phase angle becomes "Negative" (Phase Delay). In the middle of these two points the circuit is at its resonant frequency, (fr) with the two signals being "in-phase" or 0^o. We can therefore define this resonant frequency point with the following expression.

Wien Bridge Oscillator Frequency

$$f_r = \frac{1}{2\pi RC}$$

- Where:
- fr is the Resonant Frequency in Hertz
- R is the Resistance in Ohms
- C is the Capacitance in Farads

The other part, which forms the series and parallel combinations of R and C forms the feedback network and are fed back to the non-inverting input terminal (positive or regenerative feedback)

via the RC Wien Bridge network and it is this positive feedback combination that gives rise to the oscillation. The RC network is connected in the positive feedback path of the amplifier and has zero phase shift a just one frequency. Then at the selected resonant frequency, (fr) the voltages applied to the inverting and non-inverting inputs will be equal and "in-phase" so the positive feedback will cancel out the negative feedback signal causing the circuit to oscillate. The voltage gain of the amplifier circuit MUST be equal too or greater than three "Gain = 3" for oscillations to start because as we have seen above, the input is 1/3 of the output. This value, ($Av \geq 3$) is set by the feedback resistor network, R1 and R2 and for a non-inverting amplifier this is given as the ratio 1+(R1/R2). Also, due to the open-loop gain limitations of operational amplifiers, frequencies above 1MHz are unachievable without the use of special high frequency op-amps.

Procedure:-

1. Make the connection as show in fig.
2. Connect the +15v to pin no-7 of IC 741 and -15v to pin no-4.
3. Observe output at CRO and calculate resultant frequency.
4. Calculate error % of oscillated frequency.

Precautions:

1. Make sure connection of circuit is proper as circuit diagram.
2. The connection should be tight.
3. Measure the output frequency exactly.

Observation:

Wien Bridge Oscillator Frequency

$$f_r = \frac{1}{2\pi RC}$$

- Where:
- fr is the Resonant Frequency in Hertz

- R is the Resistance in Ohms
- C is the Capacitance in Farads

$$\text{Error \%} = \frac{\text{Theoritical frequency- practical frequency}}{\text{Theoritical frequency}} \times 100$$

Result: The wein bridge oscillator has been design and verified with calculation of oscillation frequency.

EXPERIMENT NO.5

HARTLEY OSCILLATOR

AIM: To determine the frequency of oscillations of Hartley oscillator.

APPARATUS: 1. BC 107 Transistor,

2. Potentiometer 10KΩ (1),

3. Resistors – 10KΩ (1), 22KΩ (1) & 100Ω (1),

4. Capacitors –10µf(2), 100µf(1) & 470pf(1),

5. Inductor 100µH (1),

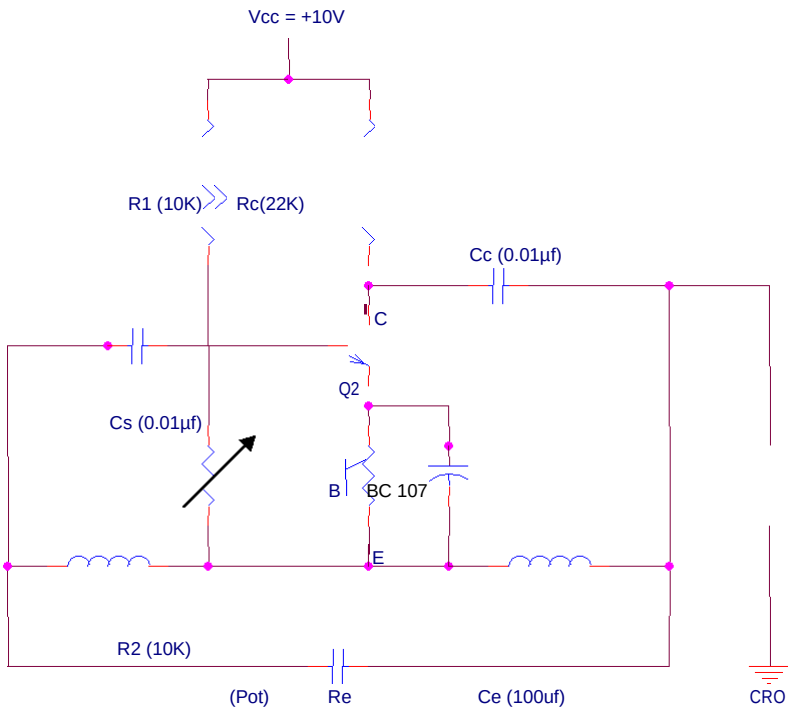
6. Decade Inductance Box (2),

7. TRPS,

8. Bread Board and connecting wires,

9. CRO with probes

CIRCUIT DIAGRAM :



PROCEDURE:

1. Connections are made as shown in circuit diagram.
2. The inductor 'L_2' is up to some value, keeping inductor 'L_1' constant.
3. The potentiometer 'R_2' is adjusted until sinusoidal waveform is observed on CRO.
4. The time period and hence the frequency are calculated for the wave obtained which is nearly equal to the theoretical frequency.
5. The experiment is repeated for different values of 'L_2' and each time the time period is noted.

TABULAR FORM:

C	Inductance			Theoretical	Time	PRACTICAL
	L_1	L_2	$L_{eq} = L_1 + L_2$	$f = 1/2\Pi\sqrt{L_{eq} C}$	T (Sec)	f = 1 /T (Hz)
470pf	3mH	3mH				
470pf	3mH	4mH				
470pf	3mH	5mH				

PRECAUTION 1. Avoid loose contacts.

2. Avoid wrong connections

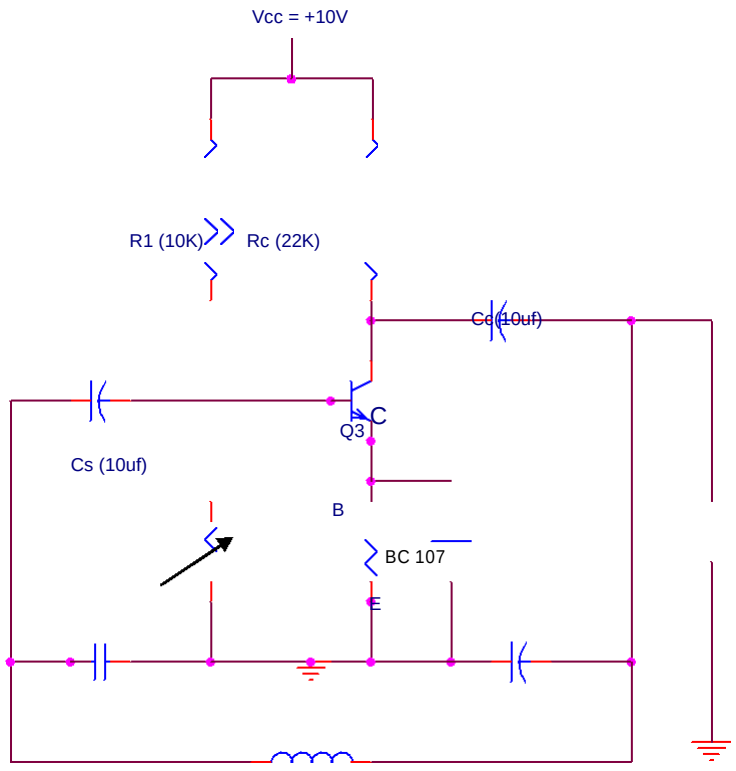
XPERIMENT NO. 6
COLPITTS OSCILLATOR

AIM: To determine the frequency of oscillations of the Colpitts oscillator.

APPARATUS.1.Transistor BC 107,

2. Capacitors – 10µf (2) & 330pf (1) & 100uf (1),
3. Resistors – 10KΩ (1), 100Ω (1) & 22KΩ (1),
4. Inductor – 0.33mH (1),
5. Decade Capacitance Box,
6. Potentiometer – 10K (1),
7. Regulated Power Supply,
8. Bread Board & Connecting Wires.

CIRCUIT DIAGRAM :



PROCEDURE :

1. The circuit is connected as shown in figure.
2. The capacitor C_1 is kept constant and C_2 is up to some value.
3. The resistor R_2 is adjusted until sinusoidal waveform is observed on the CRO.
4. Then the time period and hence the frequency are calculated which is nearly equal to the theoretical frequency.
5. The theoretical and practical values of frequency are verified using the formula.

   $f_o = 1 / 2\Pi \sqrt{LC_{eq}}$ where **$C_{eq} = \underline{C_1C_2}/C_1+C_2$**

   f_o practical = 1 /T (Hz) T = Time period.

6. The experiment is repeated for different values of C_2.

TABULAR FORM :

S.NO.	INDUCTANCE (L)	CAPACITANCE			Theoretical $f_o=1/2\Pi \sqrt{LC_{eq}}$ (kHz)	T (Sec)	f=1/T (Hz)
		C_1	C_2	C_{eq}			
1.	2Mh	330pf	330pf				
2.	2Mh	330pf	470pf				
3.	2mH	330pf	570pf				

PRECAUTIONS : 1. Avoid loose and wrong connections.

2. The sinusoidal waveform obtained must be distortion.

3. Readings should be taken without parallax error.

RESULT

Experiment No-7

AIM To design an astable multivibrator using 555 timer

Apparatus Required:- Design kit, connecting wires, ic 555, resistance, capacitors, CRO.

Circuit diagram of Square wave generator:-

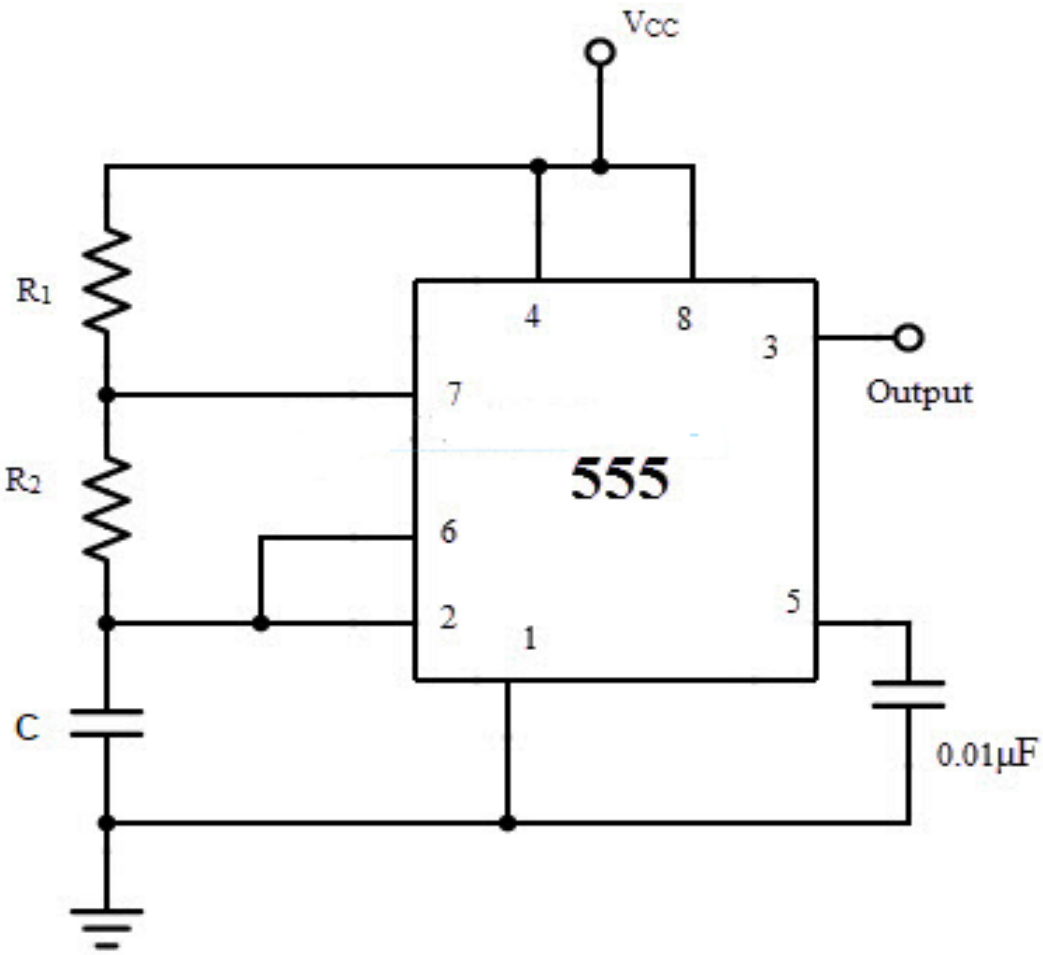


Fig Circuit diagram of square wave generator

Theory:-

Astable multivibrator is also called as Free Running Multivibrator. It has no stable states and continuously switches between the two states without application of any external trigger. The IC 555 can be

made to work as an astable multivibrator with the addition of three external components: two resistors (R1 and R2) and a capacitor (C). The schematic of the IC 555 as an astable multivibrator along with the three external components is shown below. The pins 2 and 6 are connected and hence there is no need for an external trigger pulse. It will self trigger and act as a free running multivibrator. The rest of the connections are as follows: pin 8 is connected to supply voltage (VCC). Pin 3 is the output terminal and hence the output is available at this pin. Pin 4 is the external reset pin. A momentary low on this pin will reset the timer. Hence when not in use, pin 4 is usually tied to VCC. The control voltage applied at pin 5 will change the threshold voltage level. But for normal use, pin 5 is connected to ground via a capacitor (usually 0.01µF), so the external noise from the terminal is filtered out. Pin 1 is ground terminal. The timing circuit that determines the width of the output pulse is made up of R1, R2 and C. nitially, on power-up, the flip-flop is RESET (and hence the output of the timer is low). As a result, the discharge transistor is driven to saturation (as it is connected to Q'). The capacitor C of the timing circuit is connected at Pin 7 of the IC 555 and will discharge through the transistor. The output of the timer at this point is low. The voltage across the capacitor is nothing but the trigger voltage. So while discharging, if the capacitor voltage becomes less than 1/3 VCC, which is the reference voltage to trigger comparator (comparator 2), the output of the comparator 2 will become high. This will SET the flip-flop and hence the output of the timer at pin 3 goes to HIGH. This high output will turn OFF the transistor. As a result, the capacitor C starts charging through the resistors R1 and R2. Now, the capacitor voltage is same as the threshold voltage (as pin 6 is connected to the capacitor resistor junction). While charging, the capacitor voltage increases exponentially towards VCC and the moment it crosses 2/3 VCC, which is the reference voltage to threshold comparator (comparator 1), its output becomes high.

As a result, the flip-flop is RESET. The output of the timer falls to LOW. This low output will once again turn on the transistor which provides a discharge path to the capacitor. Hence the capacitor C will discharge through the resistor R2. And hence the cycle continues. Thus, when the capacitor is charging, the voltage across the capacitor rises exponentially and the output voltage at pin 3 is high. Similarly, when the capacitor is discharging, the voltage across the capacitor falls exponentially and the output voltage at pin 3 is low. The shape of the output waveform is a train of rectangular pulses.

The formula to calculate the frequency

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$

The period is the time covered for one pulse. This is just the reciprocal of the frequency:

$$T = \frac{1}{f} = 0.69(R_1 + 2R_2)C$$

The high time (*T*1) and low time (*T*0) can be calculated using the formulas below. Note that the period is the sum of the high time and the low time.

$$T_1 = 0.69(R_1 + R_2)C$$

$$T_0 = 0.69R_2C$$

The mark space ratio is the ratio between the high time and the low time.

$$\text{Mark Space Ratio} = \frac{T_1}{T_0}$$

The formula for the duty cycle is:

$$\text{Duty Cycle} = \frac{T_1}{T} \text{ x } 100$$

A 50% duty cycle means the high time is equal to the low time. If an LED is placed at the output of this astable circuit, it will turn on at the same span of time as it is turned off. Note that getting an exact 50% duty cycle is impossible with this circuit.

Procedure:-

1. The circuit is made as shown in fig.
2. 12v supply is given to the Ic 555 timer at pin no-8 and pin no-4.
3. The output is taken across pin no-3 of IC555.
4. The output is observed at CRO and gets desired duty cycle.
5. Calculate the time period and frequency.

Result:- The square wave is generated and verified on CRO and calculation has been done.

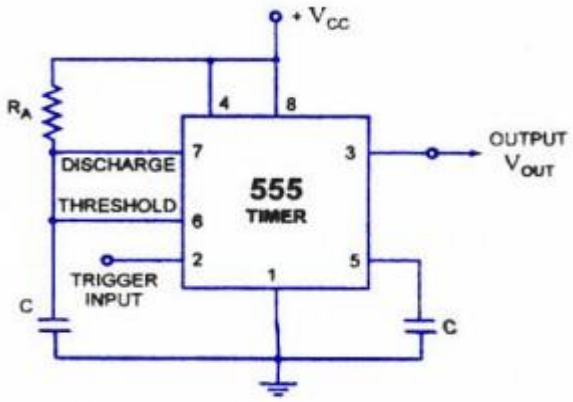
EXPERIMENT 8
MONOSTABLE MULTIVIBRATOR

AIM To design a monostable multivibrator using 555 timer

Apparatus Required: Bread board, 555 Timer, DC power supply.

Theory:

A monostable multivibrator (MMV) often called a one-shot multivibrator, is a pulse generator circuit in which the duration of the pulse is determined by the R-C network, connected externally to the 555 timer. In such a vibrator, one state of output is stable while the other is quasi-stable (unstable). For auto-triggering of output from quasi-stable state to stable state energy is stored by an externally connected capacitor C to a reference level. The time taken in storage determines the pulse width. The transition of output from stable state to quasi-stable state is accomplished by external triggering. The schematic of a 555 timer in monostable mode of operation is shown in figure.



Circuit of The Timer 555 as a Monostable Multivibrator

Pin 1 is grounded. Trigger input is applied to pin 2. In quiescent condition of output this input is kept at + V_{CC}. To obtain transition of output from stable state to quasi-stable state, a negative-going pulse of narrow width (a width smaller than expected pulse width of output waveform) and amplitude of greater than + 2/3 V_{CC} is applied to pin 2. Output is taken from pin 3. Pin 4 is usually connected to + V_{CC} to avoid accidental reset. Pin 5 is grounded through a 0.01 u F capacitor to avoid noise problem. Pin 6 (threshold) is shorted to pin 7. A resistor R_A is connected between pins 6 and 8. At pins 7 a discharge capacitor is connected while pin 8 is connected to supply V_{CC}.

Monostable Multivibrator Design Using 555 timer IC

The capacitor C has to charge through resistance R_A. The larger the time constant R_AC, the longer it takes for the capacitor voltage to reach $+2/3V_{CC}$.The RC time constant controls the width of the output pulse. The time during which the timer output remains high is given as

$$t_p=1.0986R_AC$$

where R_A is in ohms and C is in farads. The above relation is derived as below. Voltage across the capacitor at any instant during charging period is given as

$$v_c = V_{CC}(1- e^{-t/R_AC})$$

Substituting $v_c = 2/3\ V_{CC}$ in above equation we get the time taken by the capacitor to charge from 0 to $+2/3V_{CC}$.

So $+2/3V_{CC}. = V_{CC}. (1 – e^{–t/RAC})$ or $t – R_AC \log_e 3 = 1.0986\ R_AC$

So pulse width, $t_P = 1.0986\ R_AC$ s $1.1\ R_AC$

The pulse width of the circuit may range from micro-seconds to many seconds. This circuit is widely used in industry for many different timing applications.

Operation of the circuit :

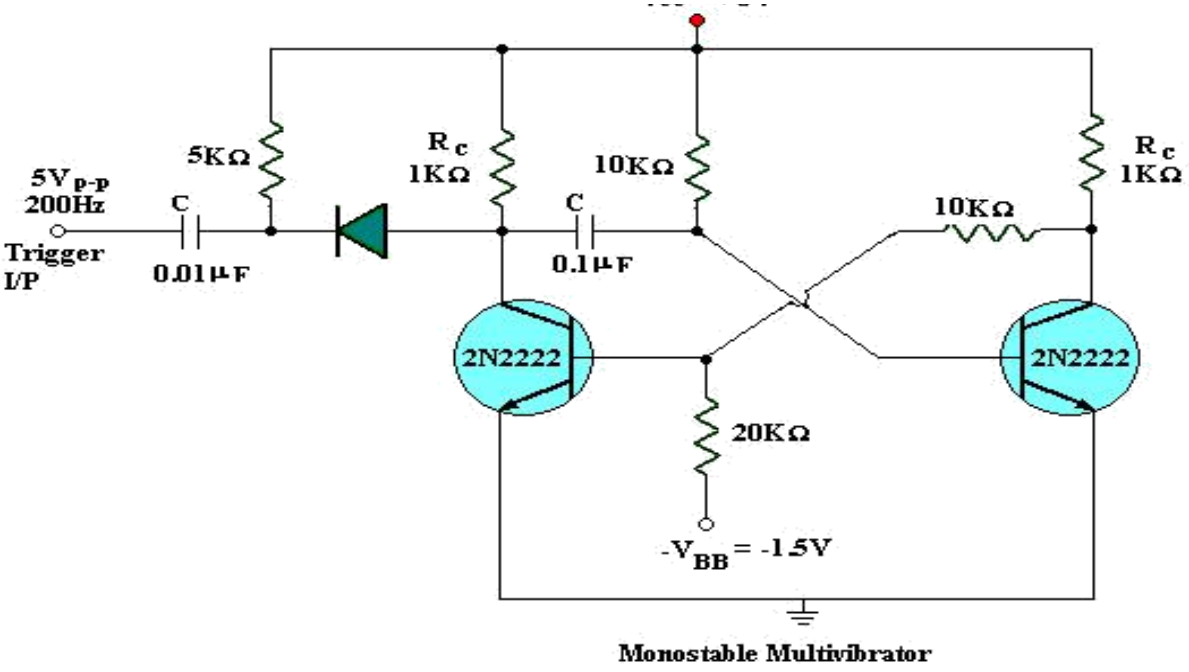
- Output of monostable 555 multivibrator remains in its stable state until it gets a trigger.
- Primarily the transistor and capacitor are shorted to ground, this state is considered as the stable state of monostable 555 multivibrator.
- As we know, when the voltage at the second pin of 555 IC goes below 1/3 Vcc, the output becomes high. This high state is known as ‘Quasi stable state’.
- The trigger causes the transition from stable state to quasi stable state.
- So when we press the button (Trigger), the voltage at 2nd pin become less than 1/3 Vcc (disconnected from Vcc) and hence the output becomes high.
- Then the discharge transistor is cut off and capacitor starts charging towards Vcc (Refer the internal circuit below). Charging of capacitor is through the resistor R1 with a time constant R1C1.
- As the capacitor voltage increases and finally exceeds 2/3 Vcc, it will reset the internal control flip flop, there by turning off the 555 timer IC (more than 2/3 voltage at the threshold pin (6th pin) causes IC to reset).
- Thus the output goes back to its stable state from Quasi stable state

Design equation for monostable multivibrator

ON time, T=1.1 R1 C1

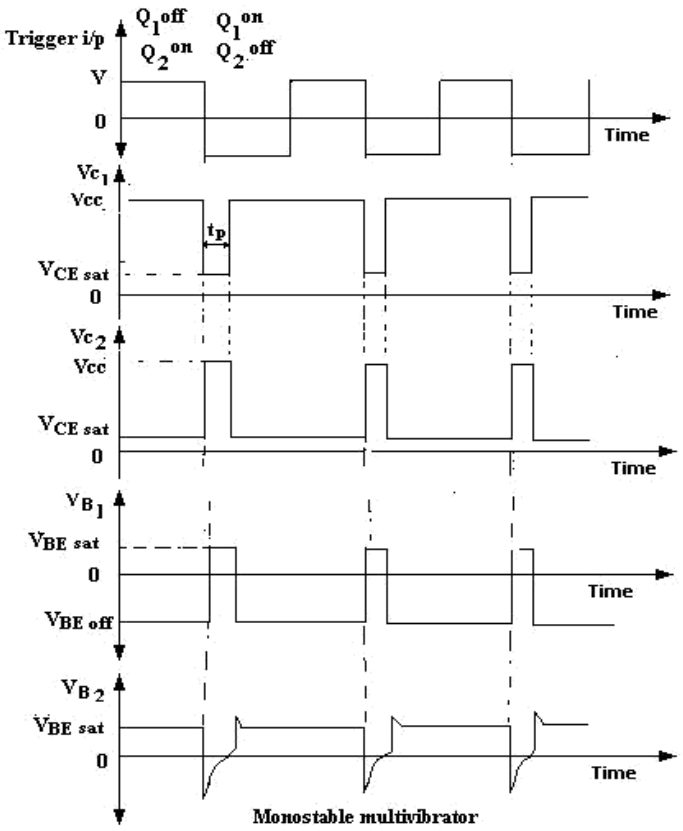
Initially, when the output is low i.e. the circuit is in a stable state, the transistor is on and capacitor- C is shorted to ground. When a negative pulse is applied to pin 2, the trigger input falls below +1/3 V_{CC}, the output of comparator goes high which resets the flip-flop and consequently the transistor turns off and the output at pin 3 goes high. This is the transition of the output from stable to quasi-stable state, as shown in figure. As the discharge transistor is cutoff, the capacitor C begins charging toward +V_{CC} through resistance R_A with a time constant equal to R_AC. When the increasing capacitor voltage becomes slightly greater than +2/3 V_{CC}, the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low, as illustrated in figure. *Thus the output returns back to stable state from quasi-stable state.* The output of the Monostable Multivibrator remains low until a trigger pulse is again applied. Then the cycle repeats. Trigger input, output voltage and capacitor voltage waveforms are shown in figure

CIRCUIT DIAGRAM:



Monostable Multivibrator

WAVEFORMS:



Applications:

- **Automatic night lamp**: We require a LDR to detect the absence of light which would then trigger them monostable multivibrator to turn the lamp on automatically.
- **Intruder Detector**: We would use the same LDR and trigger circuit as used in previous circuit along with a laser light source incident on the LDR. When some obstruction occurs the laser light would not be incident in the LDR , the monostable multivibrator circuit would be triggered and the buzzer would start to ring.

Result:

Working and applications of monostable *multivibrator has been studied*.

EXPERIMENT NO. 9

SCHMITT TRIGGER

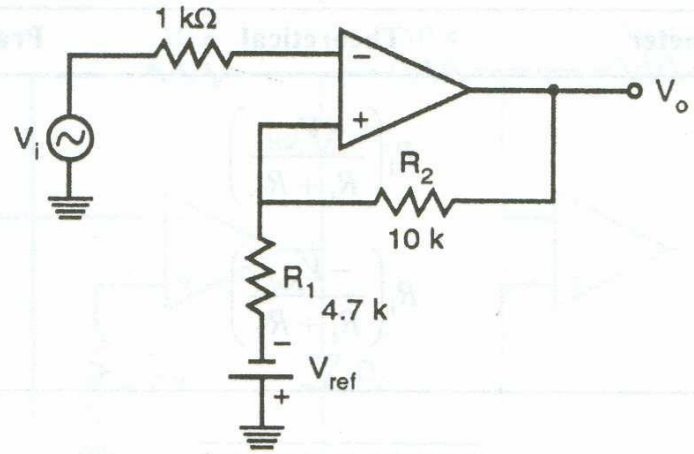
AIM: To design Schmitt trigger using Op-amp and verify its operational characteristics

APPARATUS REQUIRED:-Op-Amp – µA 741, capacitors, resistor, Dual power supply, Regulated power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. For a zero crossing detector, connect the non-inverting terminal to ground.
3. Switch on the dual power supply.
4. Observe the output waveform on the CRO
5. Draw the output and input waveforms.
6. For Schmitt Trigger set input signal (say 1V, 1 KHz) using signal generator.
7. Observe the input and output waveforms on the CRO.
8. Plot the graphs: V_i vs Time, V_O vs Time.

Schmitt trigger with negative reference

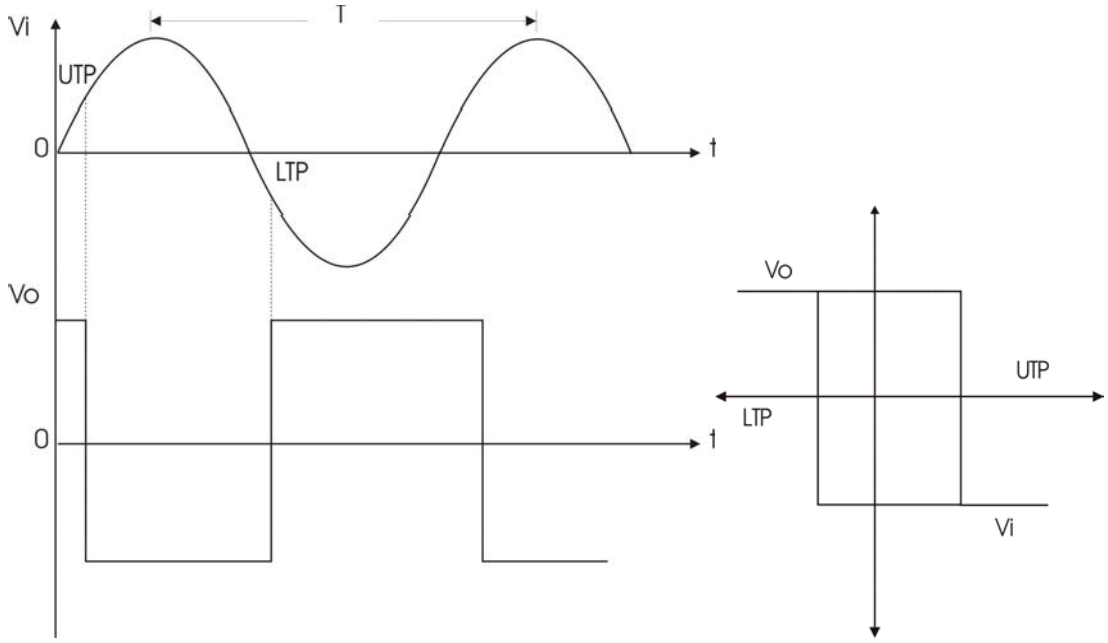


Design

Given, $V_R = 0$ and $\pm V_{sat} = \pm 12$ V.

Assume, $V_{b1} = V_{b2}$

WAVE FORMS:-



DESIGN:-

Let UTP = 6V = $\rightarrow$ $\frac{VRRI}{R1+R2} + \frac{VsatR2}{R1+R2}$

LTP = - 2V = $\rightarrow$ $\frac{VRRI}{R1+R2} + \frac{VsatR2}{R1+R2}$

Assume V_{sat} = 12V

UTP + LTP =4 = $\frac{2VRRI}{R1+R2} \rightarrow VR = \frac{2(R1+R2)}{R1} = 2(1+\frac{R2}{R1})$

UTP - LTP =8 = $\frac{2VsatR2}{R1+R2} \rightarrow VR = \frac{R1}{R2} = 2$

$\therefore$ VR = 3V, Assume R2 = 1 K fi $\rightarrow$ R1 = 2 K fi

*III*ly design for UTP = + 4, +8, +2 and -2.

LTP = - 4, + 2, - 4 and = 4

RESULT: - UTP and LTP is measured and compared with the designed value.

EXPERIMENT NO. 10

AIM: - To design and test Operational amplifier applications: (1)Inverting Amplifier, (2) Non-Inverting Amplifier, (3) Summer, (4) Voltage Follower, (5) Integrator and Differentiator.

APPARATUS REQUIRED:-

Op-Amp – μA 741, capacitors, resistor, Dual power supply, Regulated power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Give the input signal as specified
3. Switch on the dual power supply.
4. Note down the outputs from the CRO.
5. Draw the necessary waveforms on the graph sheet.
6. Repeat the procedure for all circuits.

DESIGN:-

a) Inverting Amplifier: Let Av = 10 = $\frac{Rf}{Ri}$

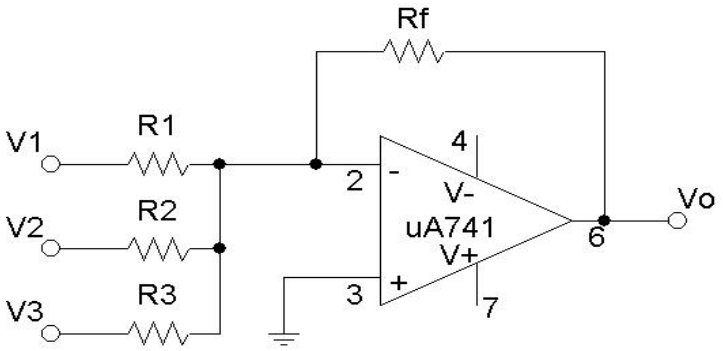
Assume Ri = 1kfi ∴ Rf = 10 Kfi, Ri = 10Kfi

b) Non Inverting Amplifier Let Av = 11 =1 + $\frac{Rf}{Ri}$

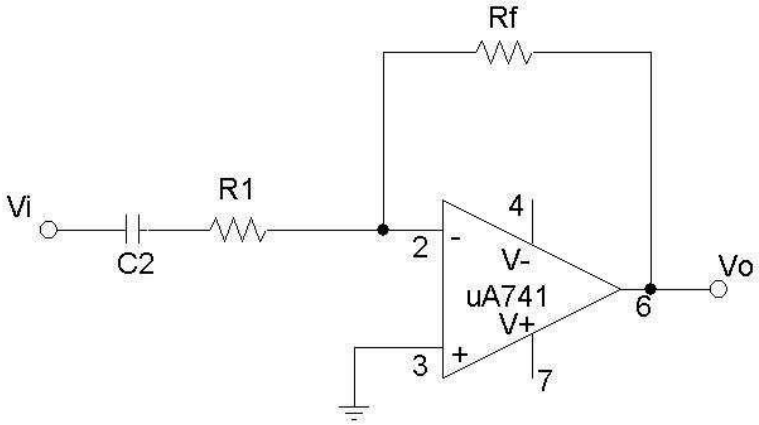
Assume Ri =1kfi ∴ Rf = (11-1) × $Ri = 10k\Omega$

c) Voltage follower Av =unity.

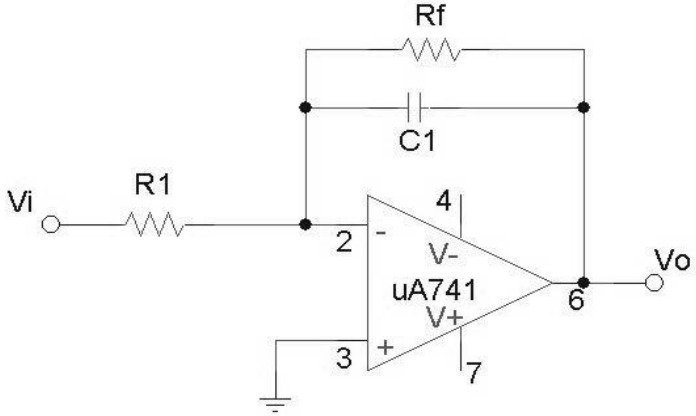
SUMMER:-



DIFFERENTIATOR:-



INTEGRATOR:-



DESIGN:-

a) Integrator

RC>>T

Let T=1msec and RC = 100 T = 100 msec

Assume R = 100 Kfi ∴C = 1μμ

Assume Rf = 10 Kfi

b) Differentiator:-

RC<<T

Let T =1msec and Rc =0.01μf Assume

R =1Kfi

c) Summer:-

$$\text{Let } Y=2V1+V2+3V3=\frac{Rf}{R1}V1+\frac{Rf}{R2}V2+\frac{Rf}{R3}V3$$

$$i.e,\ \therefore \frac{Rf}{R1}=2,\ \frac{Rf}{R2}=1 \text{ and } \frac{Rf}{R3}V3$$

Assume Fr = 10kfi ∴ R1=5Kfi, R2=10kfi and R3=3.33kfi Assume

R = 10kfi